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HIGH AND MEDIUM VOLTAGE INDUCTION MOTOR DRIVE APPLICATION WITH DIFFERENT MULTILEVEL INVERTER TOPOLOGIES

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ABSTRACT

In this paper two different multi level inverter topologies for Induction motor drive are presented. A hybrid pulse width modulation combining the merits of both space vector PWM (SVPWM) and selective harmonic elimination PWM (SHEPWM) is designed for first topology which contains neutral point clamped multilevel inverter. Another topology contains a simple cascaded H-bridge inverter with improved performance in the aspect of THD content. A comparative study and conclusion is been carried out at the end of this paper.

KEYWORDS: Multi Level Inverter, SHEPWM, SVPWM, Neutral Point Clamped Multi Level Inverter, Cascaded H-Bridge Inverter, THD

1. INTRODUCTION

WITH THE RAPID increase in the consumption of fossil fuel and electric energy, it is more desirable to develop power-electronic converters and ac drives with high efficiency, particularly in high-power applications, which play an important role in energy consumption. Different from the low-voltage applications where two-level converter dominates the market, there are several topologies available for the high-power applications, among which the three-level neutral-point-clamped (NPC) inverter is one of the most widely used topologies [1]– [5]. Compared with standard two-level inverter with the same dc-bus voltage, the three-level NPC inverter has lower voltage stress across semiconductors, less harmonic content, and more sinusoidal output voltage. Pulse width modulation (PWM) is one of the key technologies for three-level NPC inverters. So far, the PWM technologies developed for three-level inverter include multicarrier sinusoidal PWM (SPWM) [6]–[9], space-vector PWM (SVPWM) [10]–[16], and selective harmonic elimination (SHE) PWM (SHEPWM) [17]–[27], among others. For high-power applications, special attention should be paid to the low switching frequency [2], [5], [14], which is responsible for system-efficiency enhancement and for the decrease in switching loss. Different PWM techniques have different performances in terms of distribution of harmonic, total distortion, ripple characteristic, and system losses, which may affect their application range.

The SPWM for a three-level inverter can be regarded as main extension of conventional two-level SPWM by increasing the number of carriers [6]–[9]. The concept of SPWM has clear physical meaning and is easy to understand. However, conventional SPWM has low utilization of dc-bus voltage. This drawback can be overcome by injecting appropriate zero sequence component. The application of SPWM for three-level inverter drive was reported in [8], where a gate turn-off thyristor (GTO) was employed as the switching devices operating at a low switching frequency of 500 Hz. Despite the intuitive nature of SPWM, the recent digital control makes SVPWM very popular for the three-level inverter [10]–[16], which considers the inverter and motor from a system view. A synchronized SVPWM with waveform

symmetries aimed for high-power drives is proposed in [14], which is reported to have better performance than synchronized SVPWM without symmetries or SPWM with synchronization and symmetry. Recently, a simple and efficient SVPWM has been proposed in [12] for multilevel converters, which is reported to have very low computational cost while achieving similar performance to previous space-vector modulation (SVM) techniques.

II. PRINCIPLE OF SHEPWM FOR THREE-LEVEL INVERTER

The main circuit of a three-level NPC inverter is shown in Figure 1, and there are three states for one phase output: +*U*dc/2, 0, and −*U*dc/2, with the neutral point "O" as reference.

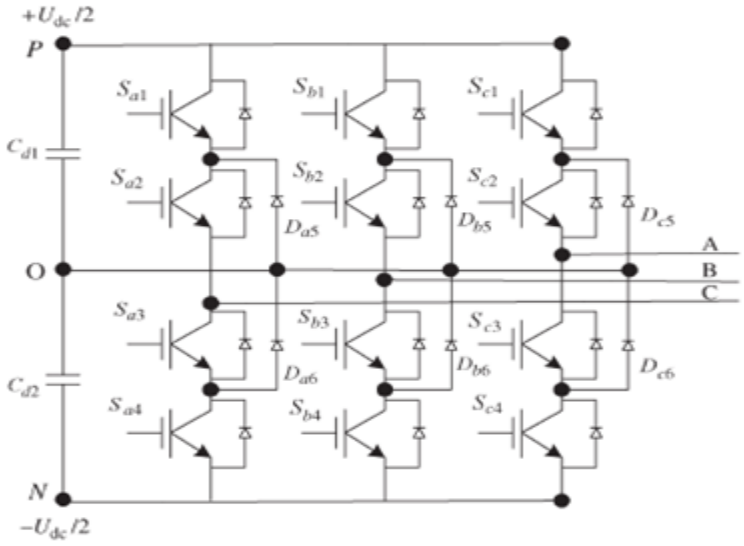


Figure 1: Main Circuit of Three-Level Inverter

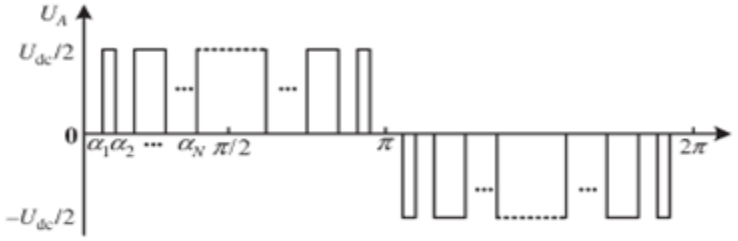


Figure 2: Typical Phase Voltage of Three-Level SHE With Quarter-Wave Symmetry

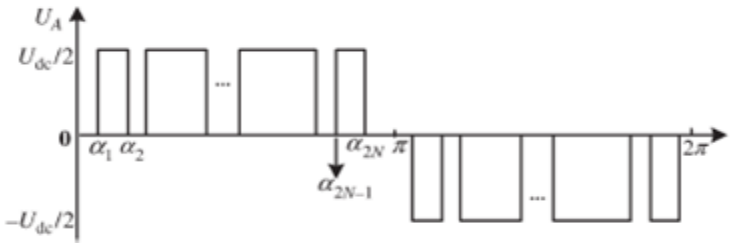


Figure 3: Typical Phase Voltage of Three-Level SHE With Half-Wave Symmetry

Conventional SHEPWM for three-level inverter assumes that the phase-voltage waveform is quarter-wave symmetric, as shown in Figure 2. This guarantees that the even harmonic will be zero, and all harmonics will be either in phase or ant iphase with the fundamental [19], [20]. Although this assumption brings some convenience, such as reduced complexity in the resulting equations, the valid solution space is limited In fact, from the view of harmonic elimination,

half-wave symmetry is enough to ensure that there will be odd-order harmonic only, so the assumption of quarter-wave symmetry is obsolete [20], [27]. The phase voltage for three-level SHEPWM without quarter wave symmetry is shown in Figure 3. for Figure 2 with a quarter wave symmetry, there are *N* angles to be solved, while there are 2*N* angles for Figure 3 with half-wave symmetry only. For symmetric three-phase system, the triple-order harmonic will cancel each other automatically in the line voltage, so it is only necessary to eliminate the non triple-order harmonics. Figure 2 can be regarded as a special case of Figure 3. The Fourier analysis of the phase voltage in Figure 3 is expressed as

$$\begin{aligned} U_A &= \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \\ &= \sum_{n=1}^{\infty} c_n \sin(n\omega t + \varphi_n) \end{aligned} \tag{1}$$

Where

$$a_n = \frac{2}{n\pi} \frac{U_{\mathrm{dc}}}{2} \sum_{k=1}^{2N} (-1)^k \sin(n\alpha_k) = c_n \sin\varphi_n \tag{2}$$

$$b_n = \frac{2}{n\pi} \frac{U_{\mathrm{dc}}}{2} \sum_{k=1}^{2N} (-1)^{k+1} \cos(n\alpha_k) = c_n \cos\varphi_n. \tag{3}$$

The modulation index in this paper is defined as $m = c1/(U\mathrm{dc}/2)$. The non triple odd-order harmonics are to be eliminated, which result in the following:

$$\begin{cases} \sum_{k=1}^{2N} (-1)^k \sin(n\alpha_k) = \frac{\pi}{2} m \sin\varphi_n, & n = 1 \\ \sum_{k=1}^{2N} (-1)^k \cos(n\alpha_k) = \frac{\pi}{2} m \sin\varphi_n, & n = 1 \\ \sum_{k=1}^{2N} (-1)^k \sin(n\alpha_k) = 0, & n = 5, 7, 11 \ldots \\ \sum_{k=1}^{2N} (-1)^k \cos(n\alpha_k) = 0, & n = 5, 7, 11 \ldots \end{cases} \tag{4}$$

Where $0 < \alpha 1 < \alpha 2 < \cdots < \alpha 2N-1 < \alpha 2N < \pi$. The maximum value for n is $3N - 2$ when n is odd number; otherwise, it is $3N - 1$ for even number of n. Under further assumption of quarter-wave symmetry as in the

Classical SHE (shown in Figure 2), the switching angles have the following relationship:

$$\alpha_k = \pi - \alpha_{2N+1-k} \tag{5}$$

Therefore, the cosine component *an* in (1) will be zero, which means that all harmonics are in phase or antiphase with the fundamental component, depending on the sign of *bn*. The equations in (4) is then simplified as

$$\begin{cases} \sum_{k=1}^{N} (-1)^{k+1} \cos(n\alpha_k) = \frac{\pi}{4} m, & n = 1 \\ \sum_{k=1}^{2N} (-1)^k \cos(n\alpha_k) = 0, & n = 5, 7, 11 \ldots \end{cases} \tag{6}$$

$$\text{where } 0 < \alpha_1 < \alpha_2 < \cdots < \alpha_N < \pi/2.$$

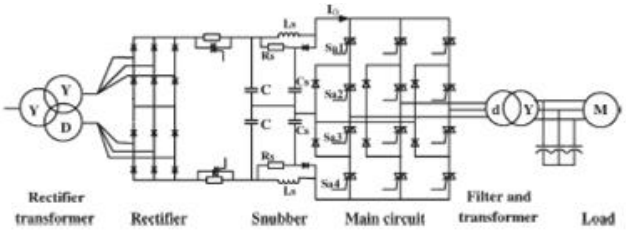
By comparing (4) and (6), it is seen that the phase of the fundamental wave $\phi 1$ is free to vary if the quarter-wave symmetry is eliminated.

III. HYBRID PWM AND SMOOTH SWITCHING:

As introduced in Section I, to combine the merits of SVPWM and SHEPWM and minimize their respective disadvantages, it is more appropriate to employ SVPWM at low frequency and SHEPWM at high frequency, which is the so-called hybrid PWM in this paper. The three-level ASD was developed for

Driving a high-power pump in a power plant. According to the specific operating requirement in the field, the ASD is mainly running in the range of 45–50 Hz to achieve high system efficiency. Considering the characteristics of SVPWM and SHEPWM, SHEPWM is designed to operate in the range of 45–50 Hz (m = 0.98−1.04), and SVPWM is employed for frequency below 45 Hz [31]. To reduce the inverter losses and increase the system efficiency, the switching frequency of SVPWM is 300 Hz (sampling frequency of 600 Hz), and the number of switching angles for SHEPWM is 7 (315–350 Hz switching frequency). In the operating range of 45–50 Hz, the

Line-voltage harmonics under at least 45 × 23 = 1035 Hz will be eliminated by SHEPWM. The remaining high-frequency harmonics can be easily filtered, so the volume of filters can be reduced compared with that using SVPWM only [32]. It should be noted that the selection of seven switching angles is related to the specific operating range required by the application. If SHE is extended to a lower output frequency, the switching angles should be increased to maintain harmonic performance.



Main circuit of 6-kV/1250-kW three-level ASD.

Figure 4

The main circuit diagram of the three-level ASD equipped with IGCTs is shown in Figure (4). To be motor friendly, the output inverter voltage is filtered before feeding the motor. The details regarding the design of filter were introduced in [32]. Both filtered and unfiltered voltages and currents obtained from experiments will be presented.

IV. PRINCIPLE OF SVPWM FOR THREE-LEVEL ASD

There are various specific implementations of three-level SVPWM [10]–[16]. In this paper, the method introduced in [33] is employed. As can be seen from Figure 5, there are six sectors for the three-level SVPWM, and each sector is divided into six regions. By taking sector 1 as an example, when the reference vector $\boldsymbol{V}^*$ falls into a certain region, such as region 2, the durations of *ta*, *tb*, and *tc* for $\boldsymbol{V}$ 1, $\boldsymbol{V}$ 2, and $\boldsymbol{V}$ 3 can be obtained based on the principle of volt–second balance, which is expressed as

$$t_a + t_b + t_c = T_s \tag{10}$$

$$\boldsymbol{V}_1 t_a + \boldsymbol{V}_2 t_b + \boldsymbol{V}_3 t_c = \boldsymbol{V}^* T_s. \tag{11}$$

Solving (10) and (11), the durations of each vector can be obtained as

$$t_a = \left(1 - \sqrt{3}m\sin\theta\right)T_s$$

$$t_b = \left[\sqrt{3}m\sin\left(\frac{\pi}{3}+\theta\right) - 1\right]T_s$$

$$t_c = \left[1 - \sqrt{3}m\sin\left(\frac{\pi}{3}-\theta\right)\right]T_s$$

Where m is the modulation index (the same meaning as defined in SHEPWM), θ is the angle of the reference voltage vector, and Ts is the sampling period.

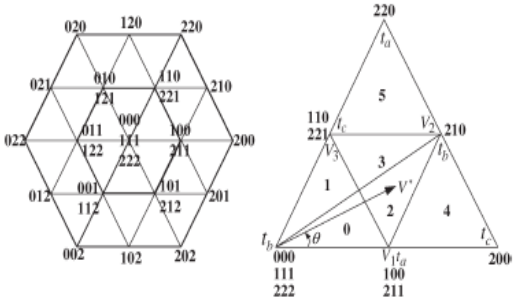


Figure 5

V. CASCADED H-BRIDGE INVERTER

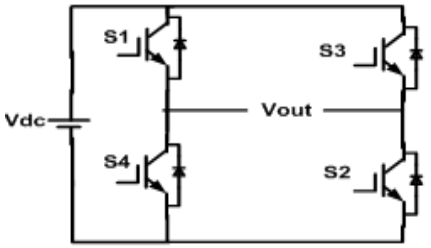


Figure 6: Circuit of the Single Cascaded H-Bridge Inverter

Figure 6 shows the circuit model of a single CHB inverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n, where n is number of H-bridges connected in cascaded. The switching sequence is given in Table 1.

Table 1

Switches Turn on	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

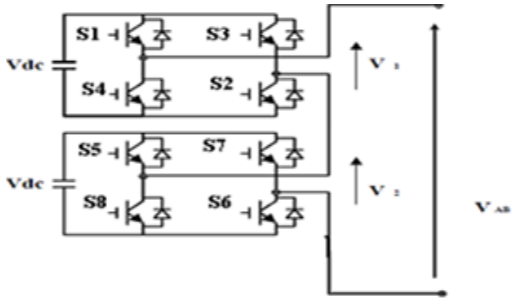


Figure 7: Block Diagram of 5-Level CHB Inverter Model

The switching mechanism for 5-level CHB inverter is shown in Table 2.

Table 2: Switching Sequence for 5-Level CHB Inverter

Switches Turn on	Voltage Level
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

PWM Techniques for CHB Inverter

The most popular PWM techniques used for CHB inverter are

- Phase Shifted Carrier PWM (PSCPWM)
- Level Shifted Carrier PWM (LSCPWM)

Case 1: Phase Shifted Carrier PWM (PSCPWM)

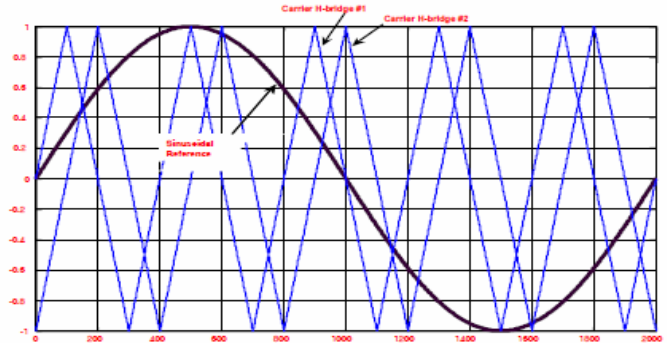


Figure 8: Phase Shifted Carrier PWM

Figure 8 shows the PSCPWM. In general, a multilevel inverter with *m* voltage levels requires (*m*–1) triangular carriers. In the PSCPWM, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by $\varphi_{cr}=360^0/(m–1)$. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for five-level inverter, four triangular carriers are needed with a 90° phase displacement between any two adjacent carriers. In this case the phase displacement of V_{cr1} = 0°, V_{cr2} = 90°, V_{cr1-} = 180° *and* V_{cr2-} = 270°.

Case 2: Level Shifted Carrier PWM (LSCPWM)

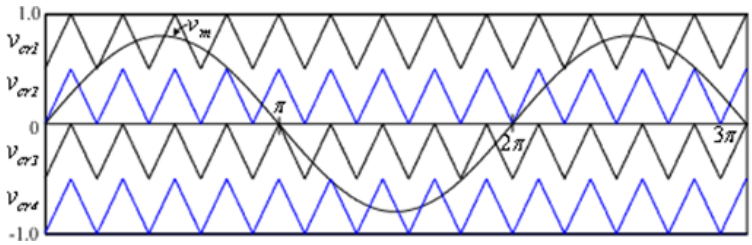


Figure 9: Level Shifted Carrier PWM (IPD)

Figure 9 shows the LSCPWM. The frequency modulation index is given by

$$m_f = f_{cr} / f_m, \quad (12)$$

Where f_m is modulating frequency and f_{cr} are carrier waves frequency. The amplitude modulation index 'm_a' is defined by

$$m_a = V_m / V_{cr} (m-1) \qquad (\text{for } 0 \leq m_a \leq 1) \qquad (13)$$

Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of the each carrier wave [1]. The amplitude modulation index, m_a is 1 and the frequency modulation index, m_f is 6. The triggering circuit is designed based on the three phase sinusoidal modulation waves V_a, V_b, and V_c. The sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs. Figures 9 and 10, 11 show the waveforms based on three schemes of LSCPWM: (a) in phase disposition (IPD) figure 9, where all carriers are in phase; (b) alternative phase opposite disposition (APOD) figure 10, where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD) figure 11, where all carriers above zero reference are in phase but in opposition with those below the zero reference [1]. Out of IPD, APOD and POD; the authors studied that, IPD give better harmonic performance.

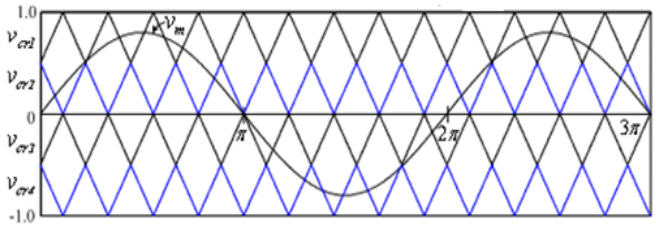


Figure 10: Alternative Phase opposite Disposition (APOD)

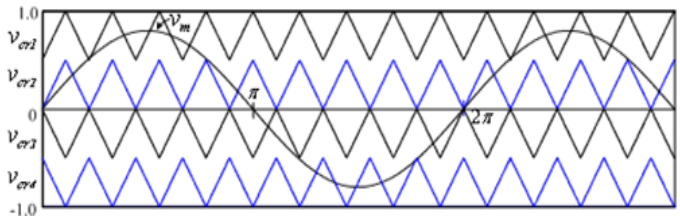


Figure 11: Phase opposite Disposition (POD)

VI.MATLAB MODELING AND SIMULATION RESULTS

Case 1*: Implementation of Proposed Concept using Neutral Clamped Type Multilevel Inverter.*

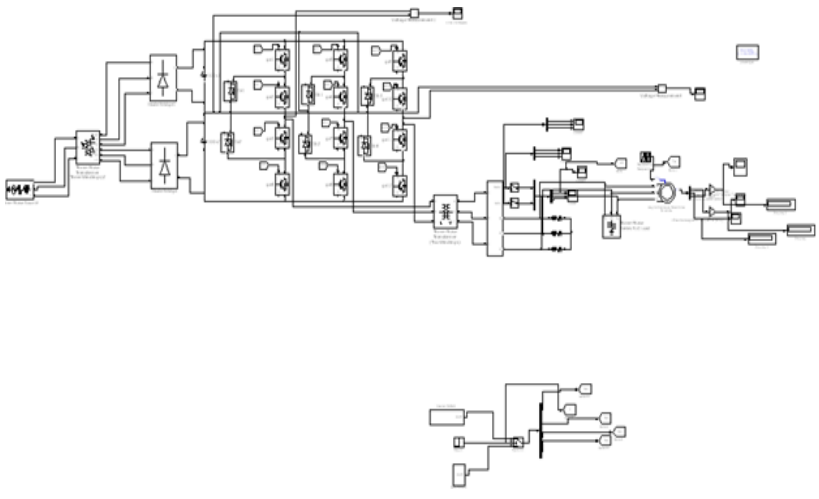


Figure 12

Phase Voltage

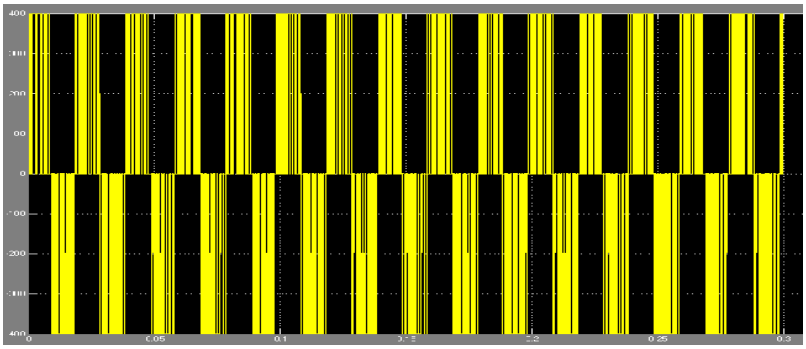


Figure 13

Line Voltage

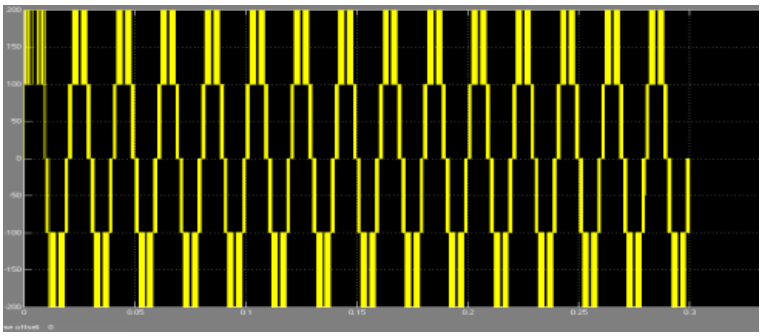


Figure 14

***Case 2**: Implementation of Proposed Concept using Cascaded H-Bridge Multilevel Type Inverter*

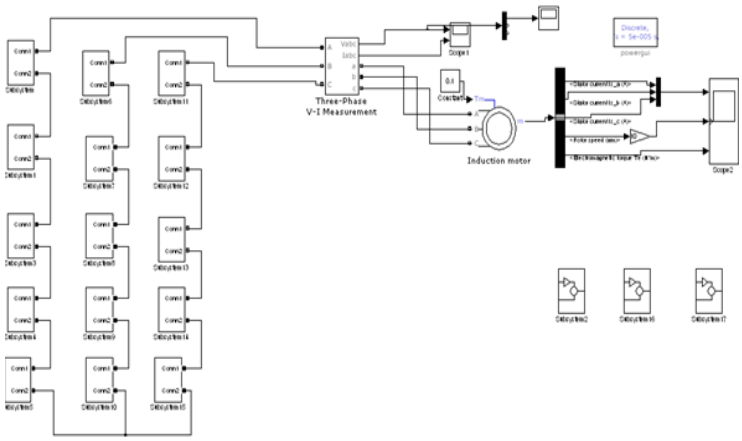


Figure 15

Phase Voltage (11 Level)

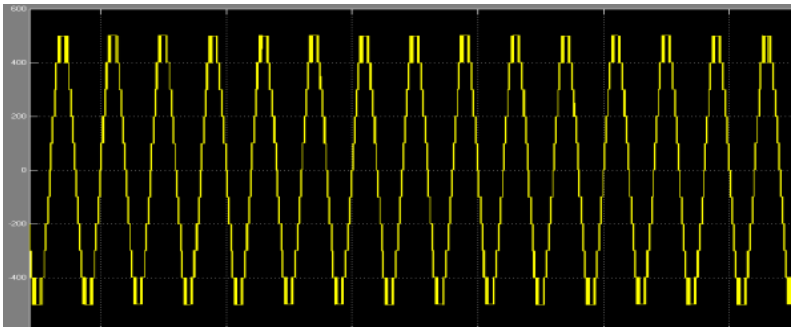


Figure 16

THD of Phase Voltage

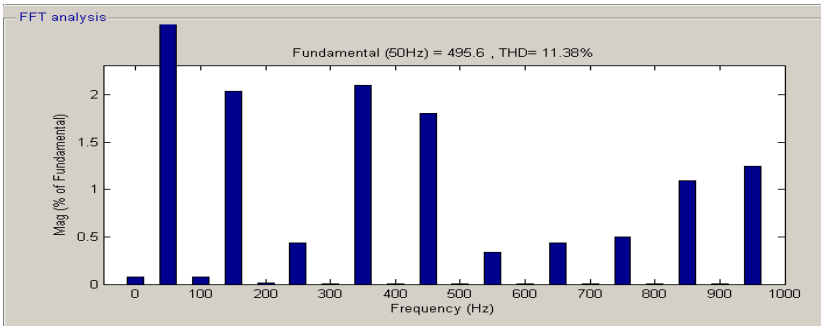


Figure 17

VII. CONCLUSIONS

This paper has presented two different topologies for induction motor drive consisting of NPC and CHB. For the topology of NPC space vector and selective harmonic eliminate modulation is used. This topology is only suited for high power industrial applications and main drawback of this topology is THD content which is in the order of 50%. So in order to suite low and medium voltage applications it is better to go for CHB topology where THD content is greatly reduced to 11%. However increasing the number of level beyond eleven is not suggested because of switching losses and economical point of view.

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